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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/642,959	08/18/2003	Giovanni Santin	400.074US02	4198

7590 06/03/2004

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EXAMINER	
TRAN, MICHAEL THANH	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 06/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/642,959	SANTIN ET AL.	
	Examiner	Art Unit	
	Michael T Tran	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *14-27* is/are allowed.

6)☒ Claim(s) *1,5,7 and 12* is/are rejected.

7)☒ Claim(s) *2-4,6,8-11 and 13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *0803*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. In response to the Communications dated August 18, 2003, claims 1-27 are active in this application.

Foreign Priority

2. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)(d), which papers have been placed of record in the file.

Information Disclosure Statement

3. The information disclosure statement filed August 18, 2003 has been considered.

Claim Objections

4. Claims 1, 5, 7, and 12 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim Rejections – 35 U.S.C. § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in-
(1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
(2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

6. Claims 1, 5, 7, and 12 are rejected under 35 U.S.C 102(e) as being anticipated by Hirano [U.S. Patent #6,198,659].

With respect to claim 1, Hirano discloses, in figure 11, a memory device, comprising: an array of floating-gate memory cells [M0-M2], each memory cell located at an intersection of a word line [WL] and a local bit line [BL0-BL2]; a first transistor [Tr] having a first source/drain region coupled to a first potential node [via WL], a second source/drain region coupled to a latch input node [at LAT0-LAT2], and a gate coupled to a first control node [rdpgen]; a second transistor [Tr0-Tr2] having a first source/drain region coupled to the latch input node [at LAT0-LAT2], a second source/drain region coupled to a first local bit line [DL], and a gate coupled to a second control node [bitsel0]; and a fuse latch [LAT0-LAT2] having an input coupled to the latch input node and an output coupled to an output node.

With respect to claim 5, Hirano discloses, in figure 11, that the floating-gate memory cell is an n-channel floating-gate field-effect transistor.

With respect to claim 7, Hirano discloses, in figure 11, that the second transistor is an n-channel field-effect transistor.

With respect to claim 12, Hirano discloses, in figure 11, that the fuse latch includes a pair of reverse-coupled inverters.

Allowable Subject Matter

7. Claims 14-27 are allowable over the prior art of record.

8. The following is an Examiner's statement of reasons for the indication of allowable subject matter: the prior art of records does not show (in addition to the other elements in the claim) the following:

- Wherein a first source/drain region of a first floating-gate memory cell is coupled to the first local bit line, a second source/drain region of the first floating-gate memory cell is coupled to a second potential node, and a gate of the first floating-gate memory cell is coupled to a first word line.
- Wherein the first transistor is a p-channel field-effect transistor.
- Wherein the first potential node is coupled to receive a supply potential.
- A latch driver circuit capable of setting an output value of the fuse latch without regard to, and without disturbing the data value of, the first floating-gate memory cell.
- A fuse latch having an input coupled to the latch input node and an output coupled to the output node; and a second logic circuit having an output coupled to the gate of the fourth field-effect transistor, a first input coupled to the third control node, and a second input coupled to the fourth control node.

Conclusion

9. When responding to the Office action, Applicants are advised to provide the Examiner with line and page numbers of the application and/or references cited to assist the Examiner in the prosecution of this case.

10. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Michael T. Tran whose telephone number is (571) 272-1795. The Examiner can normally be reached on Monday-Thursday from 7:30-6:00 P.M.

11. Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (571) 272-1650.

Michael T. Tran
Art Unit 2818
May 28, 2004